DERWENT-ACC-NO: 1981-H3898D

DERWENT-WEEK: 198132

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TITLE: Synchronising circuit digital matched filter - has input signal train clocked into shift register and pseudo-random signal shifted on switching out register feedback loop

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 771891 B	October 20, 1980	N/A	003	N/A

INT-CL (IPC): H04B003/40

ABSTRACTED-PUB-NO: SU 771891B

BASIC-ABSTRACT:

The digital matched filter is used in radio communications synchronising circuits. It operates in three stages: (i) recording the input signal train symbol into a shift register; (ii) comparison of the current code signal state of shift register (2) with a reference signal train of generator (4); and (iii) setting the scan time for the window of the pseudo-random signal train component.

At the first stage, at each clock pulse from generator (1), the binary symbol ('1' or '0') of the input signal train is read into the shift register (2) and shifts the pseudo-random signal train on switching out the feedback loop of register (2). The second stage begins with the start-up of the processing stage (8). Bul.38/15.10.80.

CHOSEN-DRAWING: Dwg.1

TITLE-TERMS: SYNCHRONISATION CIRCUIT DIGITAL MATCH FILTER INPUT SIGNAL TRAIN
CLOCK SHIFT REGISTER PSEUDO RANDOM SIGNAL SHIFT SWITCH REGISTER FEEDBACK LOOP

DERWENT-CLASS: W02

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